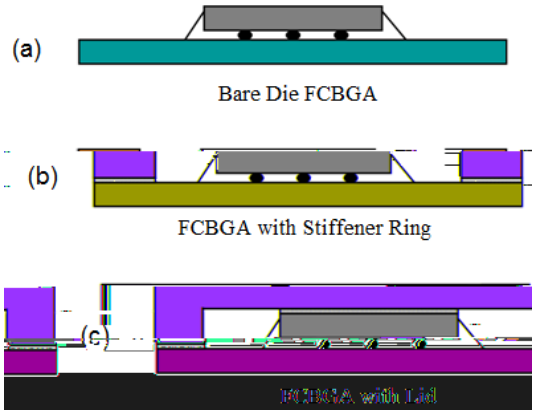
Achieving Warpage

CTE mismatch between chip and substrate is the root cause for reliability issues in flip chip packages, such as excessive warpage, low dielectric layer cracking, solder mask cracking, and bump cracking. The first and foremost thing in designing a flip chip package is to control excessive warpage to meet the specification. In this paper, a capped flip chip package is proposed to control the warpage as well as to reduce the stress. In the capped die flip chip package, a metal cap tightly covers and bonds with the die through an adhesive material. As a result, the capped die has a higher effective CTE. By adjusting the thickness of cap, the effective CTE of the capped die can match with the CTE of substrate, theoretically achieving warpage or warpage free. To verify the capped die concept for zero warpage control, 45mmx45mm sized capped die flip chip package is designed and manufactured based on the guidance from the finite element modeling, where a copper cap with 0.4mm thickness is selected. The Shadow Moiré test is performed to measure the warpage as function of temperature from 25°C to 260°C. Experimental data show that in the temperature range, the warpage curve of the capped die package is almost flat.



warpage. In Figure 2, (a), (b) and (c) show the basic assembly steps of a flip chip package, where the step (a) is for die attach process, the step (b) is for underfill dispensing and curing process, and the step (c) or (d) is for stiffener/lid attachment process. After the die attach step (a), the electrical connection between the die and substrate has been completed, and the warpage at this point is small due to the quick relaxation of the solder bump stress that is caused by the viscoplastic property of the solder material. In other words, the die attach step (a) completes the electrical connection between the die and substrate, but the mechanical connection is weak. In order to enhance the weak mechanical connection and to protect the solder bumps, the underfill is filled into the gap between the die and substrate. So, the application of underfill in the step (b) is only for the reliability of the electrical connection from the mechanical viewpoint. The underfill is usually cured at a high temperature, such as 165°C. The flip chip package during the underfill curing process is very flat, i.e., the warpage at the point is very small due to the same reason as the viscoplastic property of the solder material. However, after the underfill is cured, the die and substrate are strongly connected from mechanical viewpoint. Then, when cooling down to the room temp or rising up to the reflow temperature, the warpage will be developed due to the big CTE difference between the die and substrate. For example the downwards warpage at room temperature (also called coplanarity issue) is shown in Figure 2 (b). JEDEC specification has defined 8mil or 200um for large flip chip packages as the tolerance limit. However, for a 45mmx45mm size of flip chip package, a bare die FCBGA can have a warpage over 12mil or 300um. The excessive warpage may cause a lot of issues in board level of operations, such as solder ball bridging or opening during surface mount process, failures during package functional test. To reduce the warpage, a stiffener ring or a lid is conventionally applied in the next processing step after underfill curing process, as showed in Figure 1 (b) or (c). The mechanism of using a stiffener or lid to reduce the warpage is illustrated in Figure 2 (c) and (d) where the stiffener or lid applies a force or torque at the edge of the substrate, forcing it to deform upwards. So, it is seen that the conventional ways using a stiffener or lid to reduce the warpage is a way to deform the substrate, or says it is a substrate control method. As a result, the stress level in the flip chip package rises when the substrate is deformed by the stiffener or lid. For example, for the FCBGA with 45mmx45mm substrate size and 23mmx23mm die size, the warpage at room temperature are about 12mil, 8mil and 5mil for the package types of bare die, stiffener and lid, respectively. Though the Lidded FCBGA gives the lowest warpage, it causes highest stress in package, as compared to the bare die and stiffener packages.

In summary there are three points about the warpage control by using stiffener or lid that need to be kept in mind: (1) warpage has been developed after underfill dispensing and curing process. This means that warpage has been frozen in the package; (2) stiffener or lid attach process is done after underfill curing process; and (3) the conventional ways using stiffener or lid to control warpage is only to redeform the substrate. Therefore, the above methods are substrate control method, which will introduce an additional stress into the package.

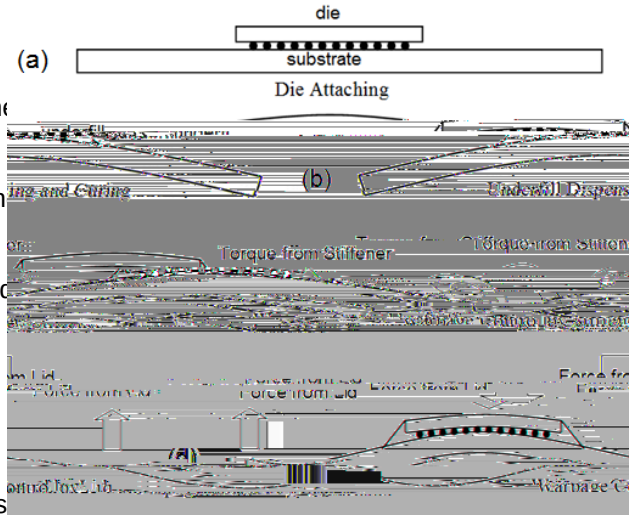


Figure 2. Assembly processes of flip chip package and mechanism of conventional ways for warpage control: (a) die attach, (b) underfill dispensing and curing, and (c) Stiffener or lid attach.

A Capped-Die Flip chip Package Design

A capped-die flip chip package is designed based on the preceding analysis for the mechanism of warpage, especially the three points of conventional warpage control mechanism, which includes a structure of capped-die flip chip package as shown in Figure 3, and an assembly process of capped-die flip chip package as shown in Figure 4. The assembly process of capped-die flip chip packages includes these steps: (a) dispensing underfill material into the gap between the die and substrate, (b) dispensing adhesive material on the top of the die, (c) covering the die cap onto the die, and (d) concurrently curing the underfill and adhesive materials.

It is seen that there are two key differences of the capped-die flip chip package design from the conventional flip chip packages using stiffener or lid. The first one is that the die cap mainly constrain the die, forming a capped die, or says it is a die control method, and the second is that the underfill material between the die and the substrate and the adhesive material between the die cap and die are concurrently cured. As a result, the CTE between the capped die and the substrate may get matched, and the warpage after the underfill dispensing and curing process as showed in Figure 2(b) may been avoided before it is frozen in the package if a die cap with a proper thickness is selected. The same base resin can give a good joint of both underfill and adhesive materials at the die edge region.

Figure 3. A capped-die flip chip package.

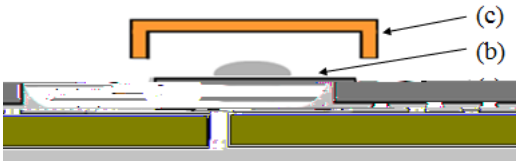


Figure 4. Assembly process for capped die flip chip package.

Some potential failure modes of a capped die flip chip packages are illustrated in Figure 5. The reason for the possible failure modes is that a high stress may take place around the die edge region when the die cap constrains the deformation of the die during temperature change. Based on this consideration, an improved die cap is designed to lessen the risk of the failure modes. The capped die flip chip packages using an improved die cap is shown in Figure 6.

Figure 5. Potential failure modes for capped die flip chip packages.

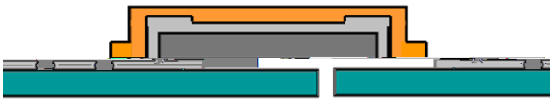
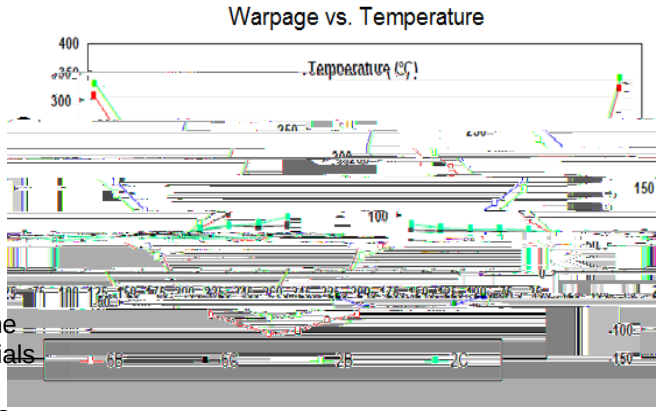


Figure 6. A capped die flip chip package using an improved die cap design.

It is suggested that the adhesive material should have the same Tg as that of the underfill material so that both materials consistently become softer or harder when temperature passes Tg. It is preferred that both materials use the same resin as their base materials, and their fillers may be different. For



under application or test loading conditions, improving the reliability of bumps and low-k layers of the package.

Finally, it is explained why the capped die package gets stable at the small warpage value 65 um. In fact, the warpage value is the warpage of the flip chip package at curing temperature 165°C. It is seen from Figure 8 that the bare die package is just having the warpage value around the temperature. The warpage value of the capped die package no

Figure 10A. Contour plot of the deformation of the big size of package at room and high temperatures.

Figure 10B. Contour plot of the deformation of the medium size of package at room and high temperatures.

Figure 10C. Contour plot of the deformation of the small size of package at room and high temperatures.

(3) Effect of the thickness of die cap

In the preceding section for achieving warpage-free packaging, the die cap thickness is selected by trial and error method through multiple rounds of simulations. Here, an interesting phenomenon, called over-controlled warpage is shown about warpage control by capped die when a thicker die cap is selected. In the simulation example, the same big package is used, but a thinner substrate core, 0.4mm thickness of core is considered. It has been seen that for 0.8mm thickness of core, 0.4mm thickness of die cap gives an ideal warpage control. The simulation shows a phenomenon of over-controlled warpage by the same 0.4mm thickness of die cap for the package with the thinner core, as shown in Figure 11(b). For the thin core, a thinner die cap, i.e., a 0.3mm thickness of die cap is proper for an ideal warpage control, as shown in Figure 11(c). Note that the conventional stiffener and lid 0 0-5(w)23(1071a)-269(0)-5(.)-2(3)-4( )-26(BT 1 0 0 1 48-4( )-26(BT 1 0 0 1 48-4(p//P << /MCa)-269(0(iv)7(es)T 1 0 07(

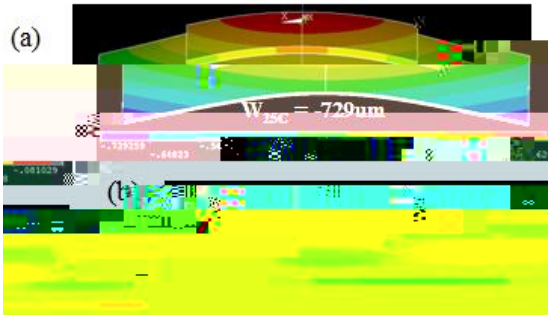


Figure 12. Contour plot of the deformation of big package using 8 layers of coreless substrate at room temperatures.

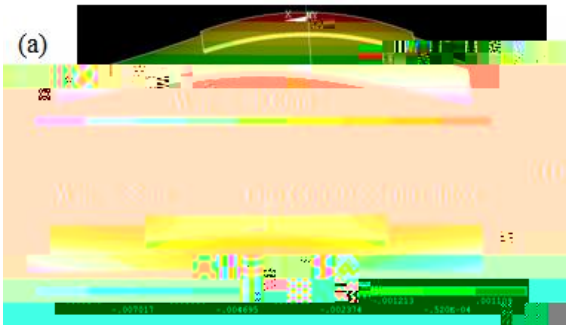


Figure 13. Contour plot of the deformation of small package using 6 layers of coreless substrate at room temperatures.

Conclusions

The experimental and simulation results show that warpage-free packaging in the full range of temperature variation can be achieved by using capped die flip chip package design. More experimental studies about the capped die flip chip package design are needed, especially for its possible failure modes. Some major design considerations include the selection of adhesive material for bonding the die cap with the die, a proper thickness of die cap, and a proper gap between the die cap side and the die edge. The assembly process needs to be carefully performed to avoid the voids between the die cap and the die because both adhesive and